IDEC Chip Design Contest

Converter Circuit for Ternary ALU Verification

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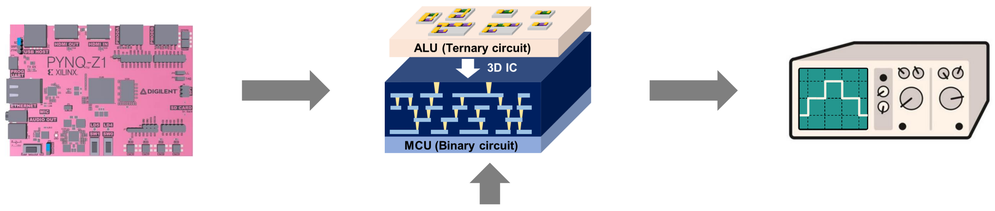
• Introduction

- Further device scaling is restricted because of power density limit.
- MVL is one of the solution.
- To verify ternary ALU, data conversion is required.

• Purpose

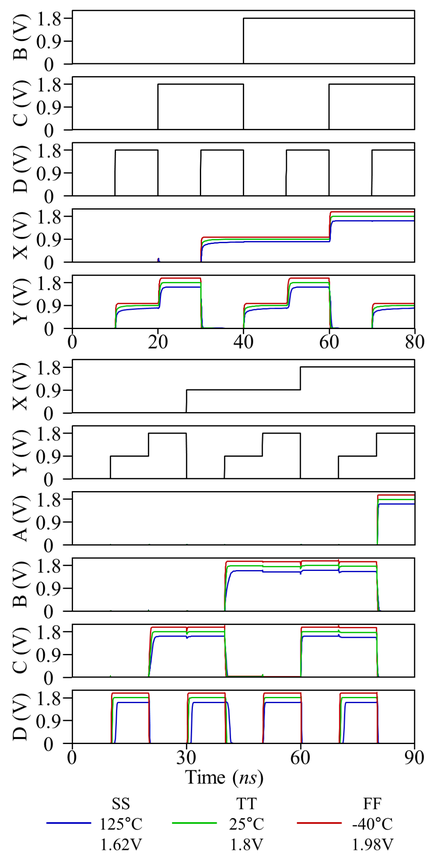
Test Pattern Generator (FPGA) → **Circuit Under Test (PCB Board)** → **Measurement (Oscilloscope)**

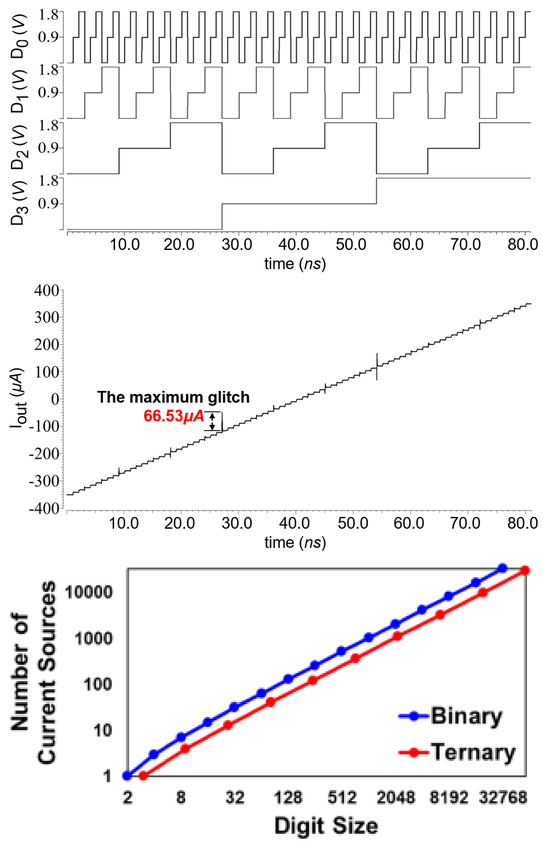


Multi-Project Wafer (MPW)

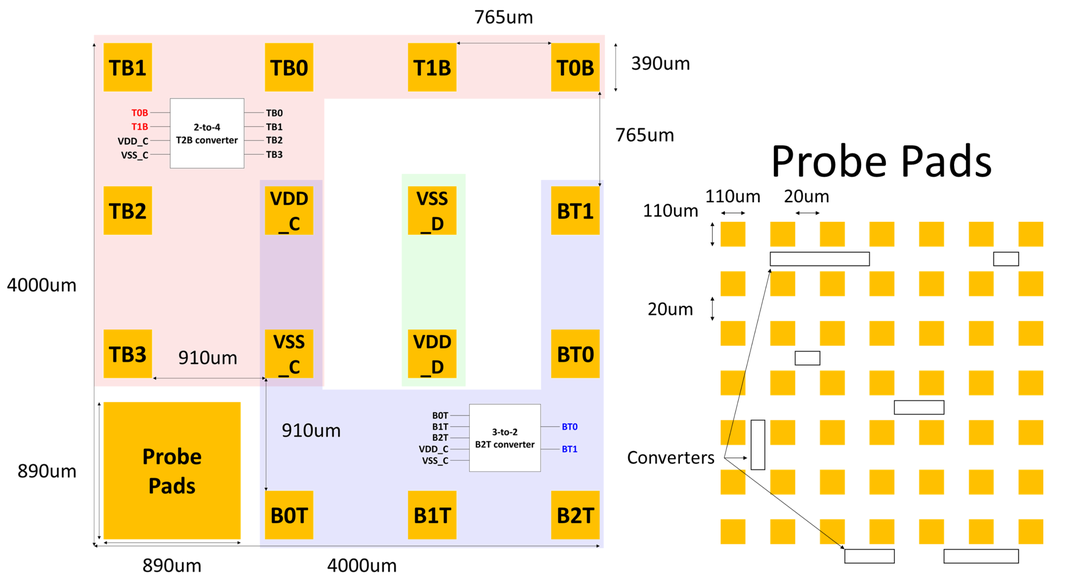
- Ternary ALU verification.
- Individual converter verification.

• Simulation Results





• Floor Plan

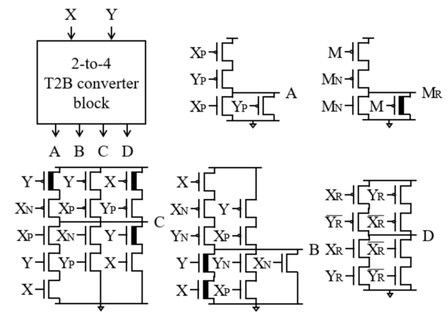


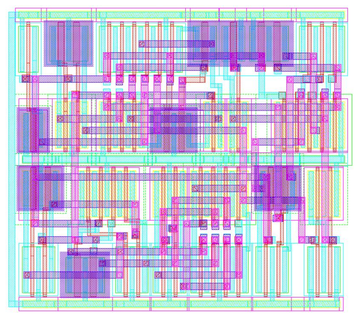
- 15 Bond pads (Ternary ALU verification)
  + Probe pads (Converters, Ternary DAC)
- Binary Input → B2T Converter → Ternary ALU → T2B Converter → Binary Output

Bondpad Size	390μm X 390μm
Bondpad Interval	910μm X 910μm / 765μm X 765μm
Probepad Array Location	(60,60)
Probepad Size	110μm X 110μm
Probepad Interval	20μm X 20μm

• Ternary to Binary Converter

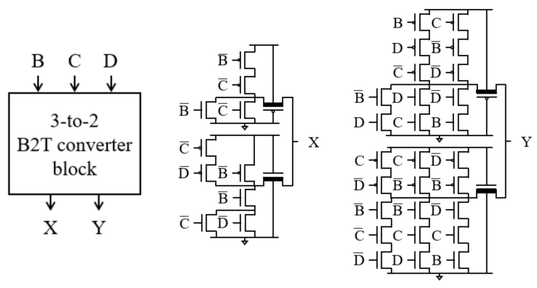
- Ternary input → Binary output
- 1-to-2, 2-to-4 T2B Converter





• Binary to Ternary Converter

- Binary input → Ternary output
- 2-to-1, 2-to-2, 3-to-2, 4-to-3 B2T Converter



• Ternary DAC